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(54) Scan velocity modulation circuit with multi-mode operation

(57) A video display deflection circuit includes a source of a video signal (Y) for displaying picture information contained in the video signal in a screen of a cathode ray tube. The video signal provides selectively on-screen-display information and non-on-screen-display information. A source of a first control signal (OSD_FLAG) has a first value, when the video signal provides on-screen-display information and a second value, when said video signal provides non-on-screen-display information. A waveform generator (63) is responsive to the first control signal for generating a second signal (63b) at a frequency that is related to a deflection frequency having a first waveform, when the video signal provides on-screen-display information, and a second waveform, that is different from the first waveform, when the video signal provides non-on-screen-display information. A modulator (31) generates a modulated correction signal (31b) by modulating, in accordance with the second signal, a time-derivative signal (30a) produced from the video signal. The correction signal is coupled to a scan velocity modulation deflection of the electron beam.

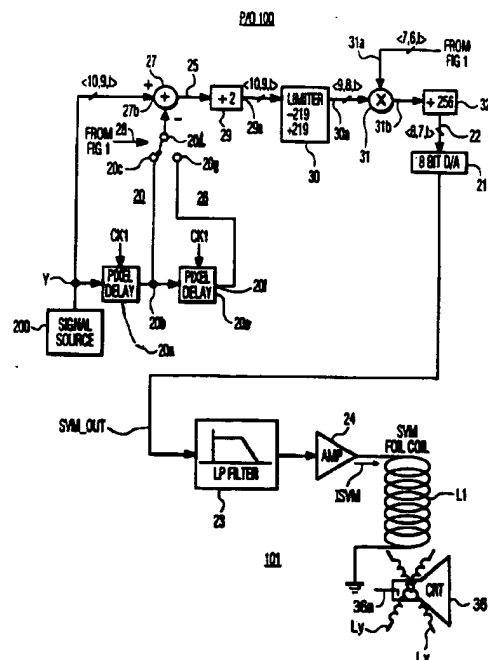


FIG. 2

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Description

[0001] The invention relates to adjusting beam scanning velocity to improve sharpness in a raster scanning display such as a cathode ray tube (CRT) display.

BACKGROUND

[0002] The sharpness of a video display may be improved by varying the horizontal scanning rate of the beam in response to variations of the luminance component of the video signal. The luminance signal is differentiated and the differentiated luminance signal is used to generate a current for driving an auxiliary beam deflection element, for example, a scan velocity modulation (SVM) coil to modify the horizontal scanning rate so as to emphasize contrast between light and dark areas of the display. For example, at a transition from black to white in a given horizontal scan line, the beam scanning speed is increased approaching the transition, thus making the display relatively darker in the black area of the transition. Upon passing the transition into the white area, the beam speed is decreased such that the beam dwells relatively longer, making the display relatively brighter. The reverse occurs in passing from light to dark.

[0003] The SVM coil operates to add or subtract from the magnetic horizontal beam deflection field applied by the main horizontal deflection coils. The angle of beam deflection is a function of horizontal rate scanning current, generally a sawtooth current. The horizontal rate scanning current causes the beam to sweep across a horizontal raster line at a vertical position determined by a vertical rate sawtooth current, coupled to the vertical deflection coils.

[0004] The sawtooth scanning drive currents are adjusted to account for the fact that the display screen is substantially flat rather than spherical. A given amount of angular beam deflection produces a smaller linear horizontal displacement of the beam at the center of the flat screen and a greater amount at the edges of the screen, because the screen is relatively farther from the source of the beam when scanning at the edges of the screen than at the center of the screen.

[0005] It may be desirable to display, for example, on-screen-display (OSD) characters on the screen of the CRT. The SVM current is, typically, optimized for non-OSD visual content. Therefore, when OSD character is displayed on the CRT screen, the SVM current could, disadvantageously, even degrade picture sharpness for OSD visual content of the picture. In one prior art, circuitry is provided for selectively disabling normal SVM circuit operation, during OSD operation.

[0006] It may be desirable to produce a waveform for the SVM current optimized for OSD display and a different waveform optimized for non-OSD display and to select dynamically the appropriate waveform. The selection may be changed on a region-by-region basis

of the screen of the CRT, in accordance with the presence or absence of OSD visual content.

[0007] In carrying out an inventive feature, a signal indicative of the start and stop positions of OSD insertions in corresponding regions of the CRT screen is provided. The waveform used for generating the SVM current is dynamically selected, in accordance with the start and stop position indicative signal. In this way, optimization can be separately obtained for OSD and for non-OSD visual contents.

[0008] In carrying out a further inventive feature, a selection of the waveforms of the SVM control signal that is coupled to the modulator is done outside the video signal path. As explain before, the SVM control signal varies in accordance with the beam position. Thereby, advantageously, different SVM current waveforms are produced for OSD and for non-OSD visual content, respectively.

SUMMARY

[0009] In an arrangement embodying an inventive feature, a video signal provides, selectively, a first type of visual content and a second type of visual content. When each of the types of visual content is provided, horizontal scanning occurs at a first horizontal deflection frequency. A first control signal has a first value, when the video signal provides the first type of visual content and a second value, when the video signal provides the second type of visual content. A waveform generator is responsive to the video signal for generating a correction signal coupled to a deflection field producing arrangement for varying a deflection field in accordance with the video signal to produce scan velocity modulated deflection of an electron beam. The waveform generator is responsive to the first control signal for generating a first waveform of the correction signal, when the first control signal is at the first value and a different, second waveform, when the first control signal is at the second value.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010]

FIGURE 1 illustrates in a block diagram a first portion of a circuit for generating a scan velocity modulation current, embodying an inventive feature;

FIGURE 2 illustrates partially in a block diagram a second portion of the scan velocity modulation current generating circuit, embodying an inventive feature;

FIGURE 3 illustrates a graph for explaining the operation of a limiter included in the circuit of FIGURE 2; and

FIGURE 4 illustrates a graph for explaining a waveform generated in the circuit of FIGURE 1.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0011] A scan velocity modulation (SVM) current generating circuit 100 of FIGURES 1 and 2, embodying inventive features, generates from a luminance signal Y of FIGURE 2 a picture enhancement or correction signal SVM_OUT. Similar symbols and numerals in FIGURES 1 and 2 indicate similar items or functions.

[0012] Signal SVM_OUT, produced in a digital-to-analog (D/A) converter 21, is coupled via a low-pass, reconstruction filter 23 and a conventional amplifier 24 to an SVM, auxiliary deflection winding or coil L1 for generating an SVM modulation current ISVM in coil L1 mounted on a cathode ray tube (CRT) 36. In addition to winding L1, a horizontal deflection winding Ly and a vertical deflection winding Lv are mounted on CRT 36 such that the three windings produce a deflection field having a horizontal component and a vertical component, in a known manner. An electrostatic type SVM device may be used, instead of coil L1, for an electrostatic type CRT. An auxiliary deflection field produced by coil L1 is used for adding to or subtracting from a horizontal deflection field produced by main horizontal deflection coils, not shown. Reconstruction filter 23 filters out high frequency components from signal SVM_OUT caused by the discrete quantization levels in signal SVM_OUT.

[0013] The impedance of coil L1 results in a significant group delay which may be compensated by introducing an additional delay, not shown, in a video path of a cathode video signal, not shown, of CRT 36. This insures that the video signal arrives at the CRT cathode at the same time the corresponding level of modulation current ISVM of FIGURE 2 is developed in SVM coil L1.

[0014] Luminance or video signal Y of FIGURE 2 is a digital signal provided as a sequence of words representing luminance or brightness information. The words of luminance signal Y are updated in synchronization with a clock signal CK1. Signal Y is obtained from a multi-standard signal source 200. Source 200 selectively generates signal Y from, for example, an analog luminance signal component of a baseband television signal, not shown, defined in accordance with a broadcasting standard, for example, NTSC, using conventional sampling techniques and displayed at a scan rate of 1H. Scan rate of 1H represents a horizontal rate that is approximately 16KHz. Source 200 selectively generates signal Y from an NTSC signal, not shown, that is up-converted to a double scan rate of 2H. Additionally, source 200 selectively generates signal Y from a high definition or a standard definition video signal, not shown, that is defined in accordance with Advance Television System Committee (ATSC) standard. Source 200 selectively generates signal Y from a computer graphics video signal, not shown.

[0015] Signal Y, as well as other digital signals in FIGURES 1 and 2, maybe formatted as a fixed point number. The fixed point number has a fixed number of

binary digits or bits and a fixed position for the decimal point with respect to that set of bits. A given fixed point number may, for example, be either an unsigned number that is always positive or a two's complement number.

[0016] Each fixed point number in FIGURES 1 and 2 has the following format:

(total_bits, integer_bits, sign_format)

The first item total_bits, is the total number of bits used to represent the fixed-point value, including integer bits, fraction bits, and sign bit, if any. The second item, integer_bits, is the number of integer bits (the number of bits to the left of the binary point, excluding the sign bit, if any). The third item, sign_format, is a letter specifying the sign format. The letter "u" stands for an unsigned number and the letter "t" stands for a two's complement number. In the unsigned format there is no sign bit and, in the two's complement format, the leftmost bit is the sign bit. For example, the fixed point number, 0101 in binary, defined by the (4,2,t) format has the value of 2.5 in decimal.

[0017] Luminance or video signal Y of FIGURE 2 is coupled to a digital differentiator formed by a filter stage 20 operating as transversal or a comb filter, embodying an inventive feature. In filter stage 20, signal Y is delayed in a clocked delay element 20a by a delay time equal to a single period of clock signal CK1 to produce a delayed signal 20b. Delayed signal 20b is selectively coupled via a pair of terminals 20c and 20d of a selector switch 26 to an input terminal 27a of a subtractor 27, when a binary switch control signal 28 of switch 26 of FIGURE 2 is at a first state.

[0018] Delayed signal 20b is further delayed in a clocked delay element 20e by a delay time equal to the single period of clock signal CK1 to produce a further delayed signal 20f. Further delayed signal 20f is selectively coupled, instead of signal 20b, via a terminal 20g and terminal 20d of selector switch 26 to input terminal 27a of subtractor 27, when switch control signal 28 is at a second state.

[0019] The state of signal 28 is determined in a decoder stage 66 of FIGURE 1. Decoder stage 66 establishes the state of signal 28 in accordance with a state of a binary signal OSD_FLAG provided by, for example, a microprocessor or a video processor, not shown. Signal OSD_FLAG indicates start and stop pixel positions of the CRT screen within which an on-screen-display (OSD) character visual content is inserted, in a conventional manner. The term OSD character identifies herein also computer graphics or other picture scenes having sharp edge objects that may be processed with respect to SVM similarly to the way OSD character visual content is processed.

[0020] Signal OSD_FLAG is at one state in a region of the CRT screen, when the displayed pixel of signal Y contains OSD character visual content and at an opposite state in a region of the CRT screen, when the displayed pixel of signal Y contains non-OSD visual

content. Non-OSD visual content is a scene typically obtained with a camera. Whereas, OSD visual content is typically obtained from a character generator included in, for example, a television receiver.

[0021] Signal Y of FIGURE 2 is also coupled to an input 27b of subtractor 27. Subtractor 27 generates a filtered or differentiated signal 25 by subtracting the selected signal at terminal 27a from that at terminal 27b. Signal 25, containing a time-derivative, dY/dt , information of luminance signal Y provides information of a brightness transition or variation from light to dark or dark to light in a picture image produced by an electron beam in CRT 36. The time-derivative is obtained in filter stage 20 by passing in signal 25 high frequency components and filtering out low frequency components of signal Y. The transfer response of filter stage 20 is selected, in accordance with the frequency of clock signal CK1 and the state of control signal 28.

[0022] Advantageously, switch control signal 28 is at the first state for selecting single delay element 20a in filter stage 20, when signal Y containing OSD character visual content is obtained from the high definition ATSC video signal, not shown, or from computer graphics video signal, not shown. Switch control signal 28 is at the second state, selecting both delay elements 20a and 20e in stage 20, when signal Y is obtained from an NTSC video signal, not shown, containing non-OSD visual content and when signal Y is obtained from the standard definition ATSC video signal, not shown. However, in another example, depending on the visual content, it may be desirable to have control signal 28 at the second state, instead, when signal Y is obtained from the high definition ATSC video signal.

[0023] The frequency of clock signal CK1 is selected by the microprocessor, not shown. When signal Y is obtained from the NTSC video signal, not shown, the frequency of signal CK1 is 27Mhz. On the other hand, when signal Y is obtained from any of the ATSC, the computer graphics and the NTSC video signals, not shown, that are up-converted for adaptation to display at scan rate of 2H, the frequency of signal CK1 is 81Mhz.

[0024] Consequently, the transfer response of filter stage 20 for signal Y, obtained from NTSC video signal containing non-OSD visual content and displayed at the scan rate of 1H, is 6dB per octave up to a frequency of 6.75 Mhz. The transfer response of filter stage 20 for non-OSD signal Y obtained from NTSC, up-converted to scan rate of 2H video signal or signal Y obtained from ATSC video signal is 6dB per octave up to a frequency of 13.5 Mhz. The transfer response of filter stage 20 for signal Y obtained from an ATSC high definition video signal is 6dB per octave up to 20.25 Mhz.

[0025] Differentiated or high-pass filtered signal 25 is coupled via a conventional divide-by-2 scaler stage 29 for generating a signal 29a that is coupled to a limiter stage 30 for generating a signal 30a. As shown in an SVM transfer curve of FIGURE 3, the value of signal

30a varies generally linearly with that of signal Y from a limit of, for example, plus 219, when the numerical value of signal Y is positive, to a limit of minus 219, when the numerical value of signal Y is negative. Similar symbols and numerals in FIGURES 1, 2 and 3 indicate similar items or functions. These limits are selected to limit a component of signal 30a, when signal Y is at a frequency in which the transfer response of filter stage 20 is at a maximum. At the limit value, signal 30a yields maximum SVM output.

[0026] A modulation multiplier 31 receives signal 30a and a modulation control signal 31a for generating an SVM level indicative signal 31b by multiplication. Signal 31a is indicative of the beam position on the screen of CRT 36, as described later on.

[0027] Signal 31b is coupled via a conventional divide-by-256 scaler stage 32 for generating an SVM level indicative signal 22. Signal 22 is coupled to an input of digital-to-analog (D/A) converter 21 that produces analog signal SVM_OUT, referred to before, in accordance with the value of each word of signal 22. Thus, signal SVM_OUT has discrete quantization levels in accordance with the values of the sequence of words of digital signal 22.

[0028] Signal 31a causes modulation current ISVM of FIGURE 2 to vary in accordance with the beam spot position on the screen. Control signal 31a is generated in the portion of circuit 100 of FIGURE 1, described next.

[0029] A register 35 containing a signal 35a provided by the microprocessor, not shown, is representative of the total number of pixels in a given horizontal line of the CRT. Signal 35a is coupled via a divide-by-2 scaler stage 37 to an input of a subtractor 38. A counter 39 counts at the rate of clock signal CK1. Counter 39 generates a signal 39a representative of a currently displayed pixel. Signal 35a is coupled to an input of subtractor 38 and is subtracted there.

[0030] During the horizontal line, an output signal 38a of subtractor 38 varies from a positive value, representative one half of the total number of pixels in the horizontal line, to a negative value, representative one half of the total number of pixels. The value of output signal 38a crosses a zero value when the electron beam is at the center of the horizontal line. Signal 38a is coupled to an absolute value producing stage 40 that produces a signal 40a containing the absolute value of signal 38a. During the horizontal line, output signal 40a varies from a positive value, representative one half of the total number of pixels, and reaches the zero value at the center of the horizontal line. Thereafter, signal 40a varies from zero to the positive value, representative one half of the total number of pixels. Thus, signal 40a is analogous to a horizontal rate, triangular shaped analog waveform having a peak value at the center of the horizontal line. The frequency of signal 40a is determined in accordance with the scan rate, for example, 1H or 2H.

[0031] Similarly, a register 55 of FIGURE 1 containing a signal 55a provided by the microprocessor, not shown, is representative of the total number of horizontal lines in the raster of the CRT. Signal 55a is coupled via a divide-by-2 scaler stage 57 to an input of a subtractor 58. A line counter 59 generates a signal 59a representative of the horizontal line that is currently displayed on the CRT. Signal 55a is coupled to an input of subtractor 58 and is subtracted there. During a vertical sweep of the CRT, an output signal 58a of subtractor 58 varies from a positive value, representative one half of the total number of lines, to a negative value, representative one half of the total number of lines. The value of output signal 58a crosses the zero value when the electron beam is at the vertical center of the raster. Signal 58a is coupled to an absolute value producing stage 60 that produces a signal 60a containing the absolute value of signal 58a. During the vertical sweep, output signal 60a varies from a positive value, representative one half of the total number of lines and reaches the zero value at the vertical center of the raster. Thereafter, signal 60a varies from zero to a positive value, representative one half of the total number of lines. Thus, signal 60a is analogous to a vertical rate triangular shaped analog waveform having a peak value at the center of the vertical scan.

[0032] When signal Y is displayed at the scan rate of 1H, the values of signals 35a and 55a are, illustratively, established at 640 and 480, respectively. Otherwise, the values of signals 35a and 55a are, illustratively, established at 1920 and 1080, respectively.

[0033] Horizontal rate signal 40a and vertical rate signal 60a are coupled to an adder 61 for producing a sum signal 61a. Signal 61a is analogous to a horizontal rate, triangular shaped analog waveform having a peak at the center of the horizontal scan and being superimposed on a vertical rate triangular shaped analog waveform. The triangular shaped analog waveform has a peak at the center of the vertical scan. Signal 61a is coupled via a divide-by-16 scaler stage 62. Stage 62 produces a signal 62a that is coupled to an input of a slope control multiplier 63.

[0034] In carrying out an inventive feature, a register 64 produces a signal 64a having a value of, for example, 240 that is provided by the microprocessor, not shown. Signal 64a providing gain or slope information of SVM control signal 31 is used when signal Y of FIGURE 2 contains non-OSD visual content. A register 65 of FIGURE 1 produces a signal 65a having a value of, for example, 120 that is provided by the microprocessor, not shown. Signal 65a providing gain or slope control is used when signal Y of FIGURE 2 contains OSD character visual content. Signal 65a of FIGURE 1 is coupled via a selector switch 71 to an input 63a of multiplier 63, when a switch control signal 70 of switch 71 is at a first state. Signal 64a is coupled via selector switch 71 to input 63a of multiplier 63, when switch control signal 70 of switch 71 is at a second state. Similarly to sig-

nal 28, discussed before, the state of signal 70 is determined in decoder stage 66. Decoder stage 66 establishes the state of signal 70 in accordance with a state of signal OSD_FLAG. Switch control signal 70 is at the first state, when signal Y contains OSD character visual content, and at the second state, when signal Y contains non-OSD visual content. The state of signal 70 varies, in accordance with signal 70, at different regions of the CRT screen.

[0035] Multiplier 63 is analogous to an analog amplifier having a variable gain selectively controlled by the parameters contained in signals 64a and 65a, respectively. Multiplier 63 produces an output signal 63b that is coupled to an input of a subtractor 72 and is subtracted there.

[0036] In carrying out a further inventive feature, a register 73 produces a signal 73a having a value of, for example, 20160 that is provided by the microprocessor, not shown. Signal 73a providing level shifting information is used when signal Y of FIGURE 2 contains non-OSD visual content. A register 74 of FIGURE 1 produces a signal 74a having a value of, for example, 10,080. Signal 74a provides level shifting control, when signal Y of FIGURE 2 contains OSD character visual content.

[0037] Signal 74a of FIGURE 1 is coupled via a selector switch 75 to an input 72a of subtractor 72, when a switch control signal 76 of switch 75 is at a first state. Signal 73a is coupled via selector switch 75 to input 72a of subtractor 72, when a switch control signal 76 of switch 75 is at a second state. Similarly to signals 28 and 70, discussed before, the state of signal 76 is determined in decoder stage 66. Decoder stage 66 establishes the state of signal 76 in accordance with a state of signal OSD_FLAG. For example, switch control signal 76 may be at the first state, when signal Y of FIGURE 2 contains OSD character visual content, and at the second state, when signal Y contains non-OSD visual content. Subtractor 72 of FIGURE 1 produces an output signal 72b and is analogous to a variable analog level shifter selectively controlled by the values of signals 73a and 74a, respectively. Advantageously, signal 72b is coupled via a divide-by-8 scaler stage 77 to an input 78b of a conventional upper limiter 78 that produces an output signal 78a.

[0038] In carrying out an additional inventive feature, a register 79 produces a signal 79a having a value of, for example, 63 that is provided by the microprocessor, not shown. Signal 79a providing an upper limit value of signal 78a is used when signal Y of FIGURE 2 contains non-OSD visual content. A register 95 of FIGURE 1 produces a signal 95a having a value of, for example, 31 that is provided by the microprocessor, not shown. Signal 95a providing an upper limit value of signal 78a is used when signal Y of FIGURE 2 contains OSD character visual content.

[0039] Signal 95a of FIGURE 1 is coupled via a selector switch 96 to an input 78c of limiter 78, when a

switch control signal 97 of switch 96 is at a first state. Signal 79a is coupled via selector switch 96 to input 78c of limiter 78, when switch control signal 97 of switch 97 is at a second state. Similarly to signal 28, discussed before, the state of signal 97 is determined in decoder stage 66. Decoder stage 66 establishes the state of signal 97 in accordance with a state of signal OSD_FLAG. Switch control signal 97 is at the first state, when signal Y of FIGURE 2 contains OSD character visual content, and at the second state, when signal Y contains non-OSD visual content. Signal 97 may have different states when the electron beam is at different regions of the CRT screen.

[0040] When the value of divide-by-8 signal 72b is smaller than the upper limit value determined by the signal at terminal 78c of limiter 78, a change in signal 72b produces a corresponding change in signal 78a. On the other hand, when the value of divide-by-8 signal 72b is equal to or greater than the upper limit value determined by the signal at terminal 78c of limiter 78, the value of signal 78a remains constant at the upper limit. Thus, limiter 78 is analogous to an analog signal clipping stage.

[0041] Signal 78a is coupled to an input 78b of a conventional lower limiter 81 that produces modulating, gain control signal 31a, mentioned before. A register 80 generates a signal 80a having a value of, for example, 0. Signal 80a containing a lower limit value is coupled to limiter 81 for establishing the lower limit value of signal 31a. When the value of signal 78a is larger than the lower limit value determined by signal 80a, a change in signal 78a produces a corresponding change in signal 31a. On the other hand, when the value of signal 78a is equal to or smaller than the lower limit value determined by signal 80a, the value of signal 31a remains constant at the lower limit.

[0042] FIGURE 4 illustrates in a two dimensional graphical diagram the variations of the value of signal 31a of FIGURE 1 as a function of a horizontal position X of FIGURE 4 and as a function of a vertical position V of the beam spot on the face of the CRT. Similar symbols and numerals in FIGURES 1, 2, 3 and 4 indicate similar items or functions.

[0043] In FIGURE 4, the picture width for a given size of the CRT screen is normalized to be in a range of values between 0 and 240 and the picture height to be in a range of values between 0 and 135, representing a 4:3 aspect ratio. The value of signal 31a varies, in accordance with the coordinates X and V, represented by a two dimensional surface 34. Surface 34 represents an approximation of a two dimensional parabola surface. The range of values of signal 31a change within the range that cannot exceed the limits, 0 to 64. A flat portion 33 of surface 34 forms a diamond. Portion 33 illustrates the level of signal 31a, during a portion of the cycle, when upper limiter 78 of FIGURE 1 provides limiting operation.

[0044] In accordance with an inventive feature, lim-

iter 78 causes the value of signal 78a to remain constant at the upper limit. The rest of surface 34 of FIGURE 4 slopes downwards from crest portion 33. The minimum value of signal 31a cannot be smaller than the lower limit established by lower limiter 81 of FIGURE 1. Thus, lower limiter 81 establishes the minimum value and upper limiter 78 establishes the maximum value of signal 31a. The slope of surface 35 representing signal 31a of FIGURE 4 outside portion 33 is controlled by the signal at terminal 63a of multiplier 63. As explained before, signal 31a is applied to modulator or multiplier 31 of FIGURE 2 for generating modulation control signal 31a.

Claims

1. A video display deflection apparatus, comprising:

means (Lx,Ly,L1) for producing a deflection field that varies a position of an electron beam on a screen of a cathode ray tube to form horizontal lines of a raster;

a source (200) of a video signal (Y) for displaying picture information contained in said video signal in said horizontal lines, said video signal providing, selectively, a first type of visual content (OSD) and a second type (non-OSD) of visual content, such that, when each of said types of visual content is provided, horizontal scanning occurs at a first horizontal deflection frequency;

a source of a first control signal (OSD_FLAG) having a first value, when said video signal provides said first type of visual content and a second value, when said video signal provides said second type of visual content; and characterized by

a waveform generator (31) responsive to said video signal for generating a correction signal (31b) coupled to said deflection field producing means for varying said deflection field in accordance with said video signal to produce scan velocity modulated deflection of said electron beam, said waveform generator being responsive to said first control signal for generating a first waveform of said correction signal, when said first control signal is at said first value and a different, second waveform, when said first control signal is at said second value.

2. A video display deflection apparatus according to Claim 1 further characterized by, a source of a second signal (40a) at a frequency related to said horizontal deflection frequency, a source of a third signal (60a) at a frequency related to a vertical deflection frequency and a summer (61) for summing said second and third signals to produce a sum signal (61a), wherein said correction signal

(31b) is produced from said sum signal.

3. A video display deflection apparatus according to Claim 1 further characterized by, a source of a second signal (40a) at a frequency related to said horizontal deflection frequency, a source of a third signal (60a) at a frequency related to a vertical deflection frequency, a multiplier (63) responsive to at least one of said second and third signals and to said first control signal (OSD_FLAG) for generating a fourth signal (63b) having a frequency that is determined in accordance with that of said at least one of said second and third signals and a value that is determined in accordance with said first control signal, wherein said correction signal (31b) is produced from said fourth signal. 5 10 15
4. A video display deflection apparatus according to Claim 3 further characterized by, means (72) responsive to said fourth signal (63b) and to said first control signal (OSD_FLAG) for generating a fifth signal (72b) that varies in accordance with said fourth signal and that includes a first level shifting value (73a), when said first control signal is at said first value, and a second level shifting value (74a), when said first control signal is at said second value. 20 25
5. A video display deflection apparatus according to Claim 1, characterized in that said first control signal (OSD_FLAG) is at said first value when said video signal provides an on-screen-display character type of visual content and at said second value, when said video signal provides a non-on-screen-display character type of visual content. 30 35
6. A video display deflection apparatus according to Claim 1, characterized in that said first control signal (OSD_FLAG) is at said first value when said electron beam is at a first region of said screen and at said second value, when said electron beam is at a second region of said screen. 40
7. A video display deflection apparatus according to Claim 1, characterized in that said deflection field producing means (Lx,Ly,L1) selectively operates in a range of deflection frequencies and wherein said correction signal (31b) varies in accordance with the selected deflection frequency. 45 50
8. A video display deflection apparatus, comprising:
 - means (Lx,Ly,L1) for producing a deflection field that varies a position of an electron beam on a screen of a cathode ray tube; 55
 - a source (200) of a video signal (Y) for displaying picture information contained in said video signal in said screen of said cathode ray tube;

a source of a first control signal (OSD_FLAG) having a first value, when said electron beam is at a first region of said screen and a second value, when said electron beam is at a second region of said screen; and characterized by

a waveform generator (31) responsive to said video signal for generating a correction signal (31b) coupled to said deflection field producing means for varying, in accordance therewith, said deflection field to provide scan velocity modulation, said waveform generator being responsive to said first control signal for generating a first waveform of said correction signal, when said first control signal is at said first value and a different, second waveform of said correction signal, when said first control signal is at said second value.

9. A video display deflection apparatus according to Claim 8 further characterized by, a source of a second signal (40a) at a frequency related to said horizontal deflection frequency, a source of a third signal (60a) at a frequency related to a vertical deflection frequency, a multiplier (63) responsive to at least one of said second and third signals and to said first control signal (OSD_FLAG) for generating a fourth signal (63b) having a frequency that is determined in accordance with that of said at least one of said second and third signals and a value that is determined in accordance with said first control signal, wherein said correction signal (31b) is produced from said fourth signal.
10. A video display deflection apparatus according to Claim 9 further characterized by, means responsive to said fourth signal (63b) and to said first control signal (OSD_FLAG) for generating a fifth signal (72b) that varies in accordance with said fourth signal and that includes a first level shifting value (73a), when said first control signal is at said first value, and a second level shifting value (74a), when said first control signal is at said second value.
11. A video display deflection apparatus according to Claim 8, characterized in that said first control signal (OSD_FLAG) is at said first value when said video signal provides an on-screen-display character type of visual content and at said second value, when said video signal provides a non-on-screen-display character type of visual content.
12. A video display deflection apparatus according to Claim 8, characterized in that said correction signal (31b) produces scan velocity modulated deflection of said electron beam.
13. A video display deflection apparatus according to Claim 8, characterized in that said deflection field

producing means (Lx,Ly,L1) selectively operates in a range of deflection frequencies and wherein said correction signal (31b) varies in accordance with the selected deflection frequency.

14. A video display deflection apparatus, comprising:

means (Lx,Ly,L1) for producing a deflection field that varies a position of an electron beam on a screen of a cathode ray tube;
a source (200) of a video signal (Y) for displaying picture information contained in said video signal in said screen of said cathode ray tube;
means for generating a first signal (31a) that varies in accordance with the position of said beam on said screen;
a source of a clock signal (CK1); and characterized by
means (31) responsive to said video, first and clock signals for generating a binary, correction signal (31b) having a sequence of states varying in accordance with said video and first signals, said correction signal being coupled to said deflection field producing means to produce scan velocity modulated deflection of said electron beam.

15. A video display deflection apparatus according to Claim 14, characterized in that said deflection field producing means (Lx,Ly,L1) selectively operates in a range of deflection frequencies (1H, 2H) and wherein when a first deflection frequency (1H) of said deflection field is selected, a corresponding frequency of said clock signal (CK1) is selected and when a second deflection frequency (2H) of said deflection field is selected, a different frequency of said clock signal is selected in a manner to provide for multi-mode operation.

16. A video display deflection apparatus according to Claim 14, further characterized by, a source of a control, second signal (OSD_FLAG) having a first value, when said video signal provides said first type of visual content (OSD) and a second value, when said video signal provides said second type of visual content (non-OSD), said second signal being coupled to said correction signal producing means (31) for producing a first sequence of states of said correction signal (31b), when said second signal has said first value, and a second sequence of states of said correction signal, when said second signal has said second value.

17. A video display deflection apparatus according to Claim 16, characterized in that said first signal (31a) generating means is responsive to said clock (CK1) and second (OSD_FLAG) signals for producing a third sequence of states of said first signal,

when said second signal has said first value (OSD), and a fourth sequence of states of said first signal, when said second signal has said second value (non-OSD).

18. A video display deflection apparatus according to Claim 16, characterized in that said second signal (OSD_FLAG) is at said first value when said video signal (Y) provides an on-screen-display character type of visual content and at said second value, when said video signal provides a non- on- screen-display character type of visual content.

19. A video display deflection apparatus according to Claim 14, characterized in that said correction signal (31b) is coupled to an auxiliary winding (L1) to produce scan velocity modulated deflection of said electron beam.

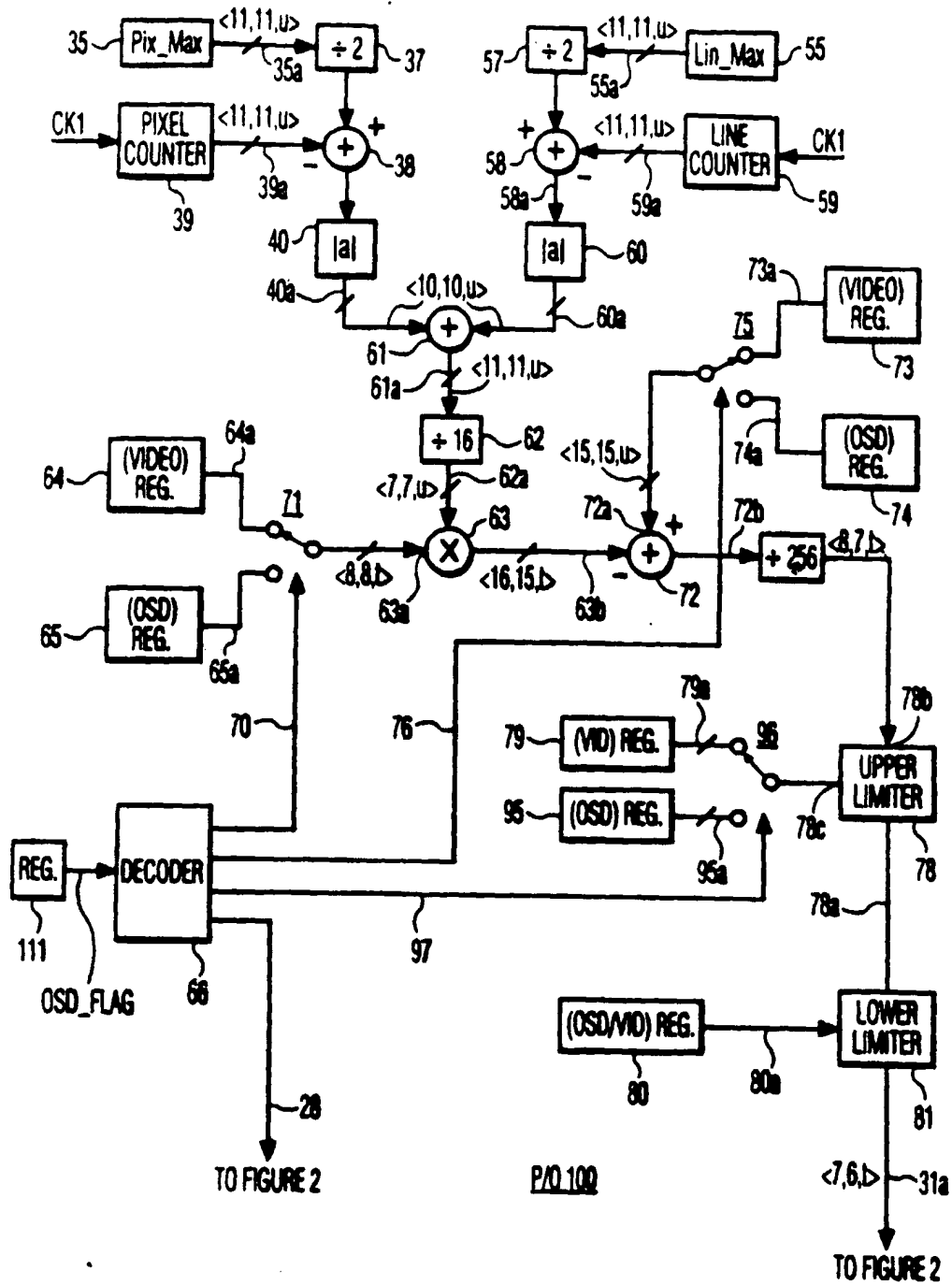


FIG. 1

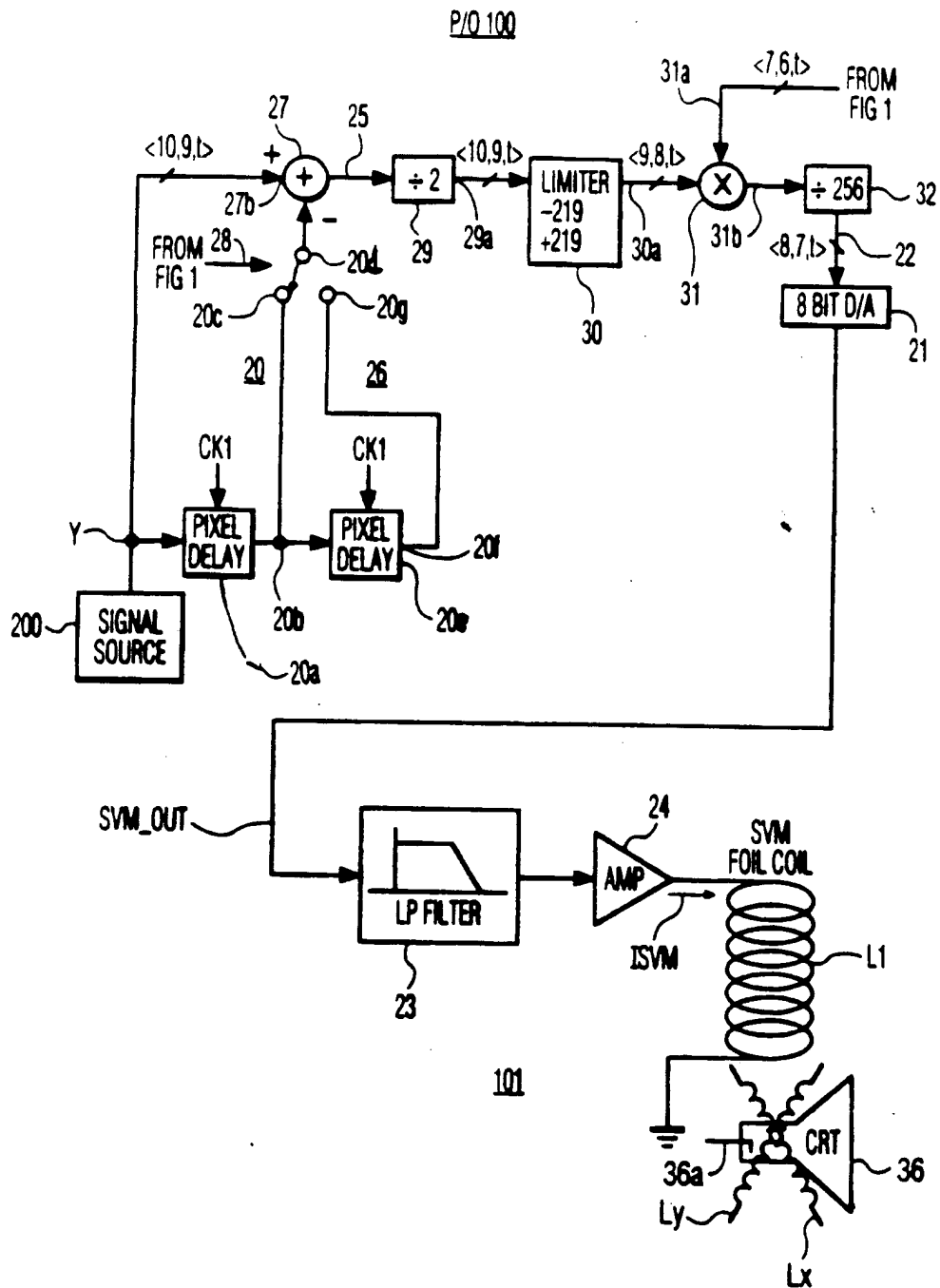


FIG. 2

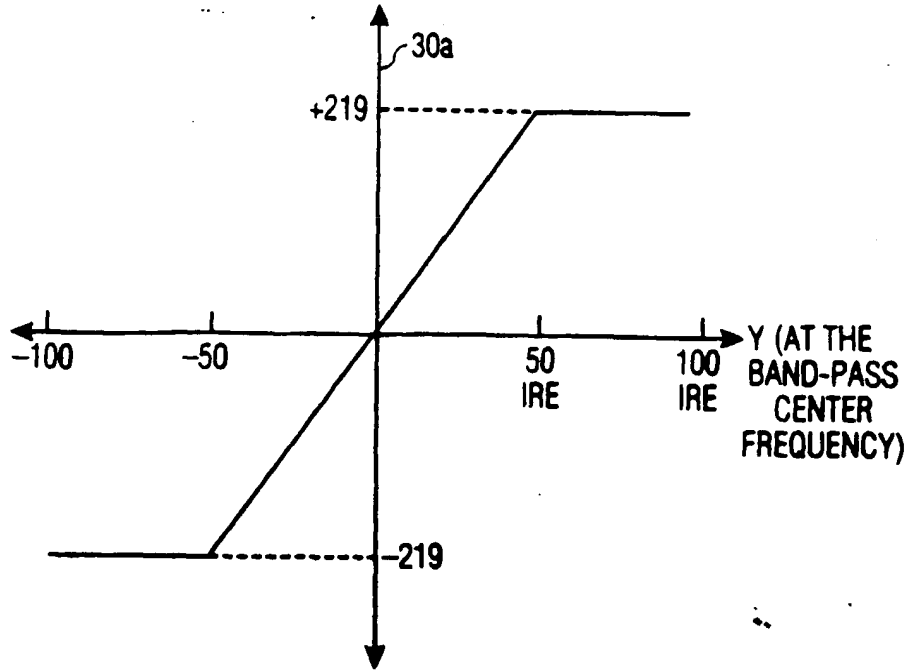


FIG. 3

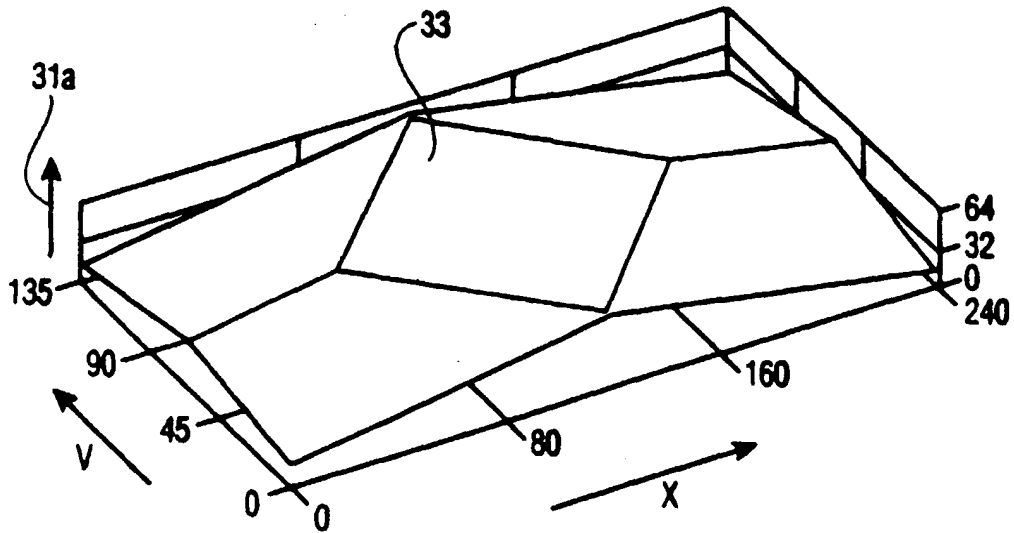


FIG. 4



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EUROPEAN SEARCH REPORT

Application Number

EP 00 11 0936

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	EP 0 472 121 A (RCA LICENSING CORP) 26 February 1992 (1992-02-26) * column 1, line 44 - column 2, line 10 * ---	1,8	H04N3/32
A	EP 0 469 567 A (THOMSON CONSUMER ELECTRONICS) 5 February 1992 (1992-02-05) * column 4, line 31 - line 40 * ---	1,8	
A	US 5 528 312 A (NO GWAN H ET AL) 18 June 1996 (1996-06-18) * column 6, line 54 - line 58 * ---	1,8	
A	PATENT ABSTRACTS OF JAPAN vol. 018, no. 580 (E-1626), 7 November 1994 (1994-11-07) & JP 06 217160 A (SONY CORP), 5 August 1994 (1994-08-05) * abstract * ---	1	
A	PATENT ABSTRACTS OF JAPAN vol. 012, no. 375 (E-666), 7 October 1988 (1988-10-07) & JP 63 123275 A (MITSUBISHI ELECTRIC CORP), 27 May 1988 (1988-05-27) * abstract * -----	7	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
			H04N
-The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 26 June 2000	Examiner BEQUET, T
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document</p> <p>T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons ----- &: member of the same patent family, corresponding document</p>			

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CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

- ☒ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

1-13

- ☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

- ☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

- ☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

- ☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

- ☒ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:



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**LACK OF UNITY OF INVENTION
SHEET B**

Application Number
EP 00 11 0936

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1-13

Control of the scan velocity modulation depending on the frequency content of the video signal (in the present case modification of the SVW for an OSD).

2. Claims: 14-19

Control of the scan velocity depending on the beam position on the screen.

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 00 11 0936

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

26-06-2000

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0472121 A	26-02-1992	CN 1059251 A,B	04-03-1992
		DE 69123202 D	02-01-1997
		DE 69123202 T	26-06-1997
		ES 2096605 T	16-03-1997
		JP 5284380 A	29-10-1993
		MX 9100731 A	01-04-1992
		PT 98727 A,B	31-01-1994
		TR 26135 A	15-02-1995
		US 5179320 A	12-01-1993
EP 0469567 A	05-02-1992	US 5072300 A	10-12-1991
		CA 2047898 A,C	03-02-1992
		CN 1058688 A,B	12-02-1992
		CS 9102371 A	19-02-1992
		DE 69116254 D	22-02-1996
		DE 69116254 T	18-07-1996
		ES 2084068 T	01-05-1996
		FI 913678 A	03-02-1992
		HK 1004315 A	20-11-1998
		HU 62127 A	29-03-1993
		JP 4245786 A	02-09-1992
		JP 11103398 A	13-04-1999
		JP 11103399 A	13-04-1999
		JP 11127365 A	11-05-1999
		PL 166499 B	31-05-1995
		PT 98536 A,B	30-09-1993
		SK 279265 B	05-08-1998
		TR 26420 A	15-03-1995
US 5528312 A	18-06-1996	JP 7087354 A	31-03-1995
JP 06217160 A	05-08-1994	NONE	
JP 63123275 A	27-05-1988	NONE	

EPO FORM PD459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82